TM2G0060065T

650V N-Channel Silicon Carbid Power MOSFET

V_{DS}	=	650 V
$R_{DS(on)}$	=	60 mΩ
I_D	=	67 A

Features

- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- Low on-resistance with high junction temperature
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Easy to parallel
- RoHS compliant

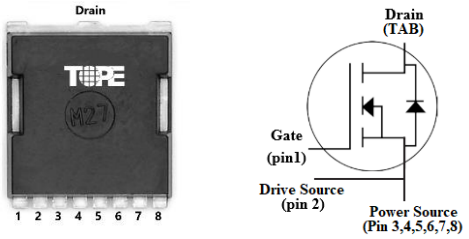
Benefits

- Higher System Efficiency
- Reduce cooling requirements
- Increased power density
- Minimize gate ringing
- Reduction of system complexity and cost

Applications

- Switch Mode Power Supplies
- DC/DC converters
- Solar Inverters
- EV charging infrastructure
- Energy storage & battery
- Battery control unit

Package



Part Number	Package	Marking
TM2G0060065T	TOLL	TM2G0060065T

Maximum Ratings, at T_J = 25℃, unless otherwise specified

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain-Source Breakdown Voltage	650	V	V_{GS} = 0 V, I_D = 100 μA	
I_D	Continuous Drain Current	67	A	V_{GS} = 20 V, T_C = 25 ℃	Fig. 18
		47	A	V_{GS} = 20 V, T_C = 100 ℃	
$I_{D(pulse)}$	Pulsed Drain Current	112	A	Pulse width t_p limited by T_{jmax}	
P_D	Power Dissipation	362	W	T_C = 25 ℃	Fig. 19
$V_{GS,op}$	Recommend Gate Source Voltage	-5/+20	V		
V_{GSmax}	Maximum Gate Source Voltage	-10/+25	V	AC（f > 1Hz)	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +175	℃		
T_L	Soldering Temperature	260	℃		

Electrical Characteristics, at T_J = 25°C, unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
Static							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650	--	--	V	V_{GS} = 0 V, I_D = 100 μA	
I_{DSS}	Zero Gate Voltage Drain Current	--	10	100	μA	V_{DS} = 650 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage	--	5	250	nA	V_{GS} = 20 V	
$V_{GS(th)}$	Gate-Source Threshold Voltage	2	--	4	V	I_D = 5 mA, V_{GS} = V_{DS}	Fig. 11
$R_{DS(on)}$	Drain-Source On-State Resistance	--	60	80	mΩ	V_{GS} = 20 V, I_D = 13.2 A	Fig. 6
			80		mΩ	V_{GS} = 18 V, I_D = 13.2 A	
			89		mΩ	V_{GS} = 15 V, I_D = 13.2 A	
Dynamic							
C_{iss}	Input Capacitance	--	1129	--	pF	V_{GS} = 0 V, V_{DS} = 600 V f = 1.0 MHz, V_{AC} = 25 mV	Fig. 17
C_{oss}	Output Capacitance	--	114	--			
C_{rss}	Reverse Transfer Capacitance	--	6.5	--			
E_{oss}	C_{oss} Stored Energy	--	25	--	μJ		Fig. 16
Q_g	Total Gate Charge	--	62	--	nC	V_{DS} = 400 V I_D = 13.2 A V_{GS} = -5/+20 V	Fig. 12
Q_{gs}	Gate-Source Charge	--	18	--			
Q_{gd}	Gate-Drain Charge	--	33	--			
$t_{d(on)}$	Turn-on Delay Time	--	21.3	--	ns	V_{DS} = 400 V V_{GS} = -5/+20 V I_D = 13.2 A $R_{G(ext)}$ = 2.5 Ω	
t_r	Turn-on Rise Time	--	14.5	--			
$t_{d(off)}$	Turn-off Delay Time	--	132.6	--			
t_f	Turn-off Fall Time	--	42.7	--			
$R_{G(int)}$	Internal Gate Resistance	--	2.8	--	Ω	f = 1.0 MHz, V_{AC} = 25 mV	

Body Diode Characteristics, at T_J = 25°C, unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
I_S	Continuous Diode Froward Current	--	--	56	A		
$I_{S(pulse)}$	Diode pulse Curren	--	112	--	A		
V_{SD}	Diode Froward Voltage	--	3.0	--	V	V_{GS} = 0 V, I_S = 6.6 A	Fig. 8, 9, 10
t_{rr}	Reverse Recovery Time	--	23	--	ns	I_S = 13.2 A, V_{DS} = 400 V V_{GS} = -5 V dif/dt = 2100 A/μs	
Q_{rr}	Reverse Recovery Charge	--	132	--	nC		
I_{rrm}	Peak Reverse Recovery Current	--	13	--	A		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	--	0.414	--	°C/W	Fig. 20

Typical Performance

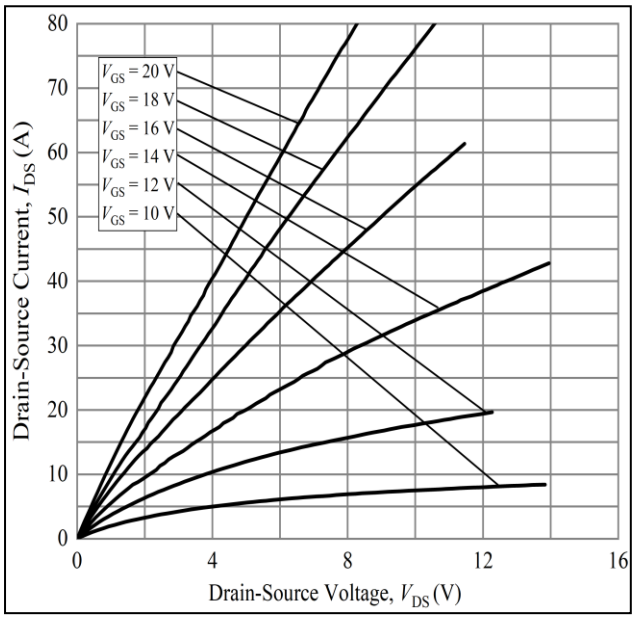


Figure 1: Typical Output Characteristics at T_J = -55 °C

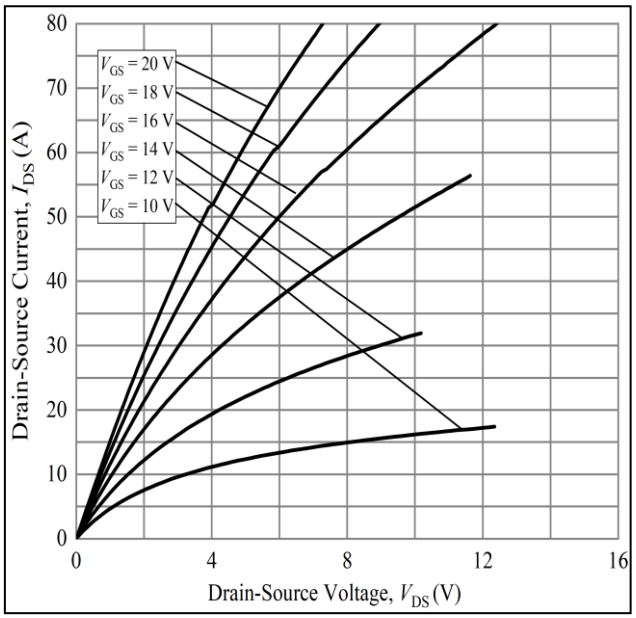


Figure 2: Typical Output Characteristics at T_J = 25 °C

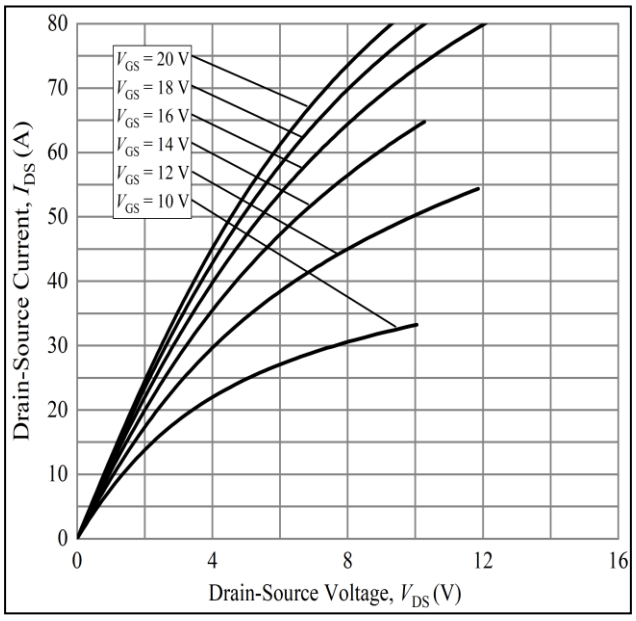


Figure 3: Typical Output Characteristics at T_J = 175 °C

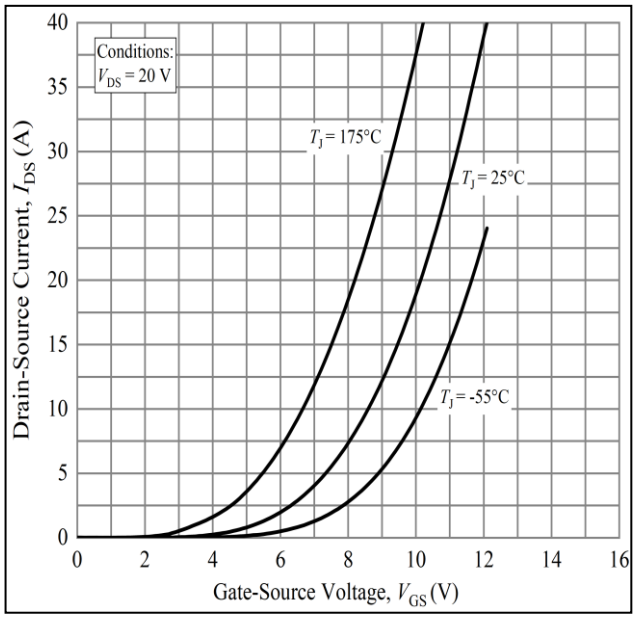


Figure 4: Typical Transfer Characteristics for Various Temperature

Typical Performance

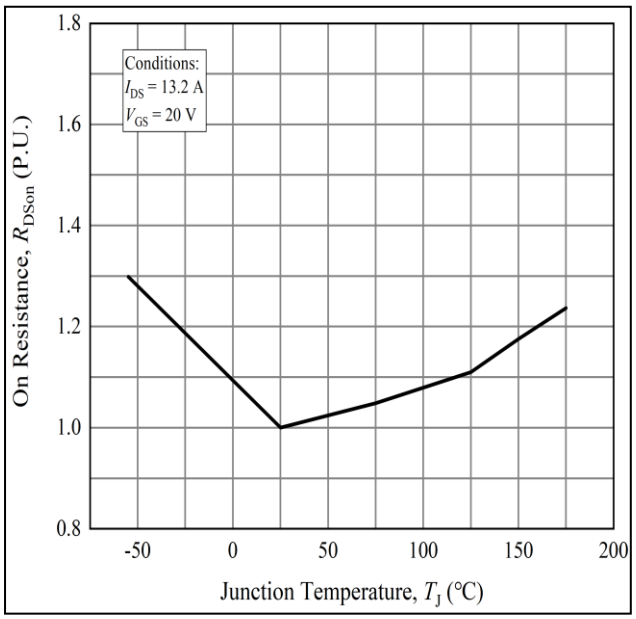


Figure 5: Normalized On-Resistance vs. Temperature

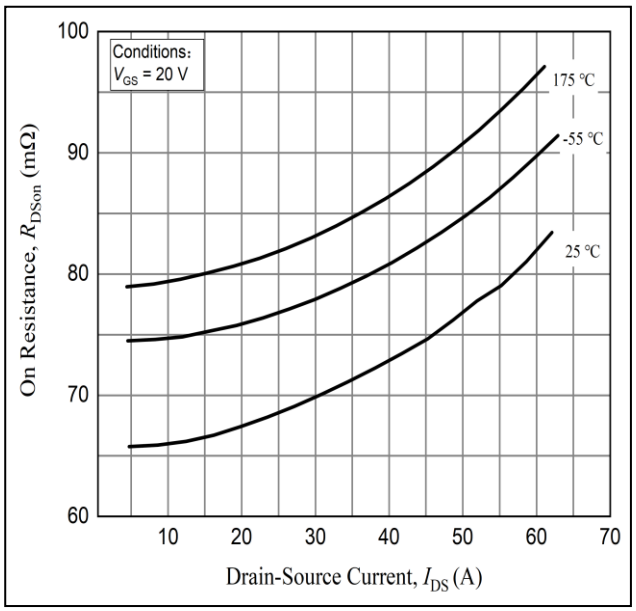


Figure 6: On-Resistance vs. Drain Current for Various Temperatures

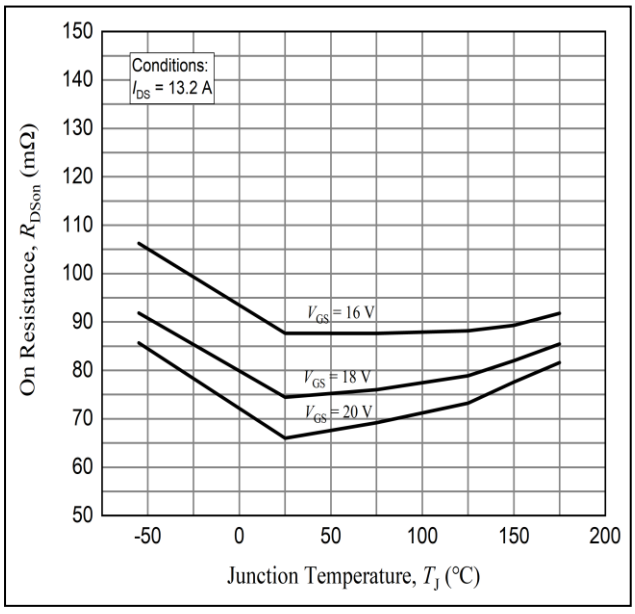


Figure 7: On-Resistance vs. Temperature for Various Gate Voltage

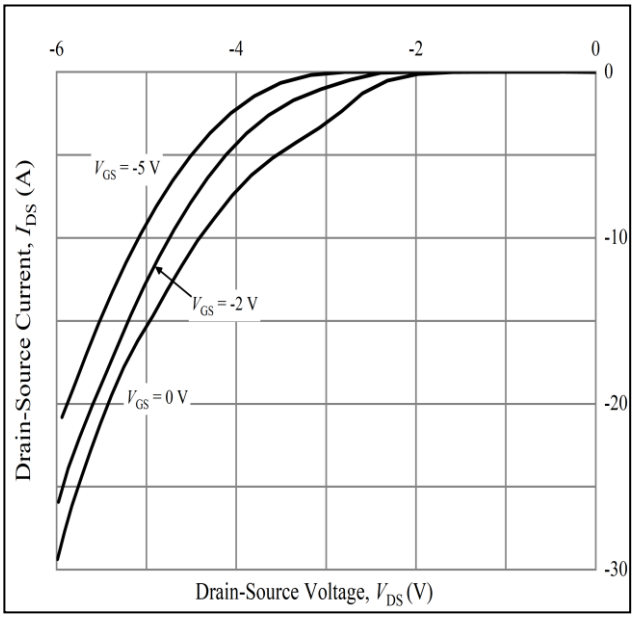


Figure 8: Typical Body Diode Characteristics at T_J = -55 °C

Typical Performance

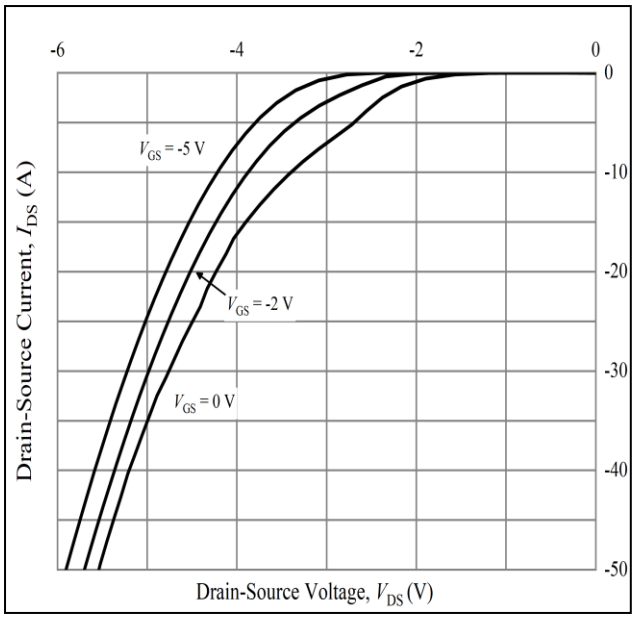


Figure 9: Typical Body Diode Characteristics at T_J = 25 °C

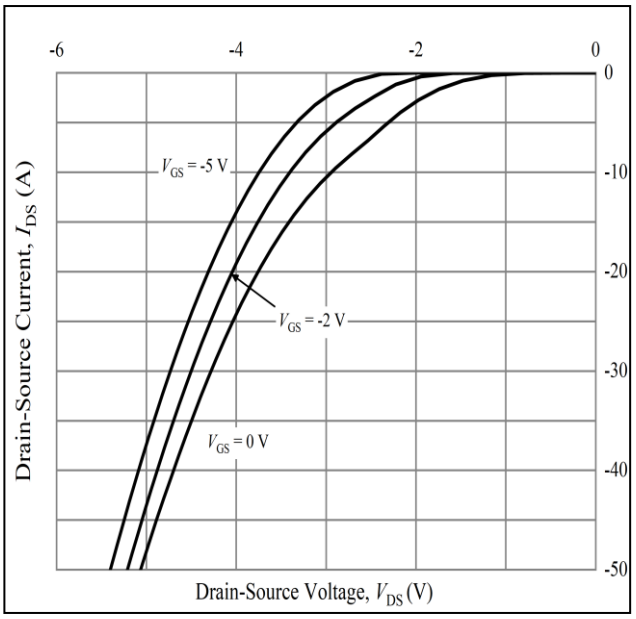


Figure 10: Typical Body Diode Characteristics at T_J = 175 °C

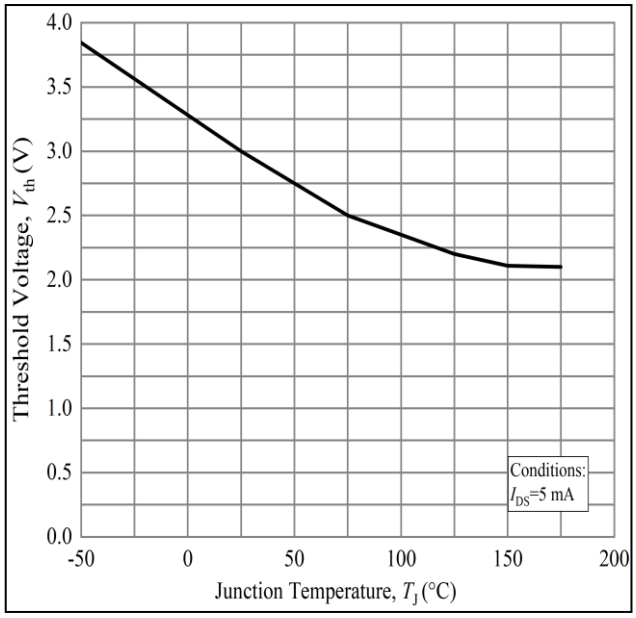


Figure 11: Typical Threshold Voltage vs. Temperature

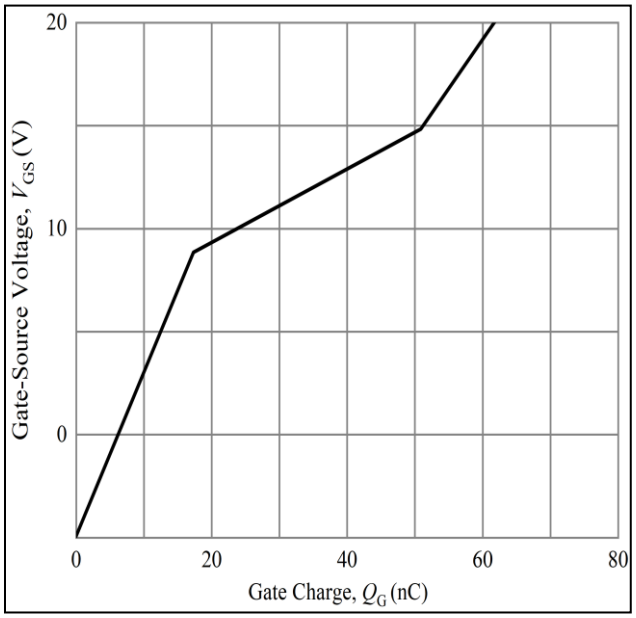


Figure 12: Typical Gate Charge Characteristics at T_J = 25 °C

Typical Performance

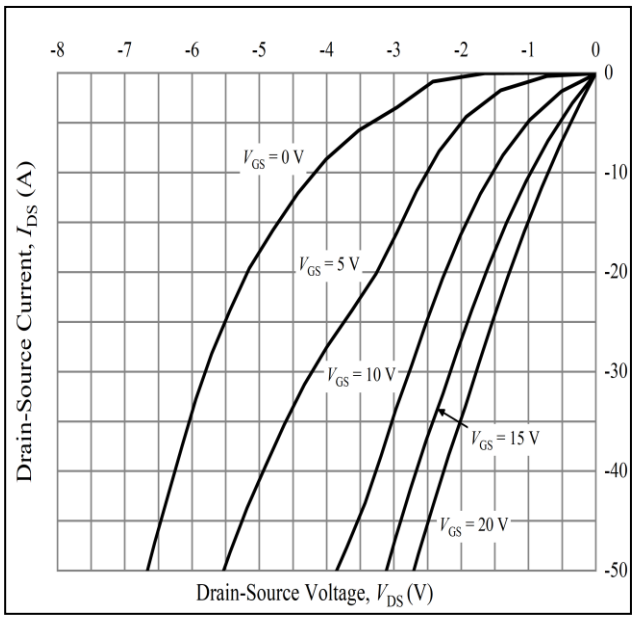


Figure 13: Typical 3rd Quadrant Characteristics T_J = -55 °C

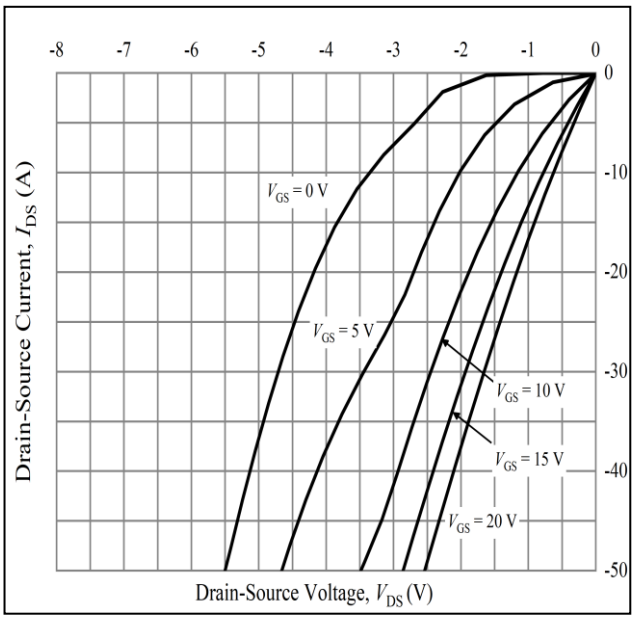


Figure 14: Typical 3rd Quadrant Characteristics at T_J = 25 °C

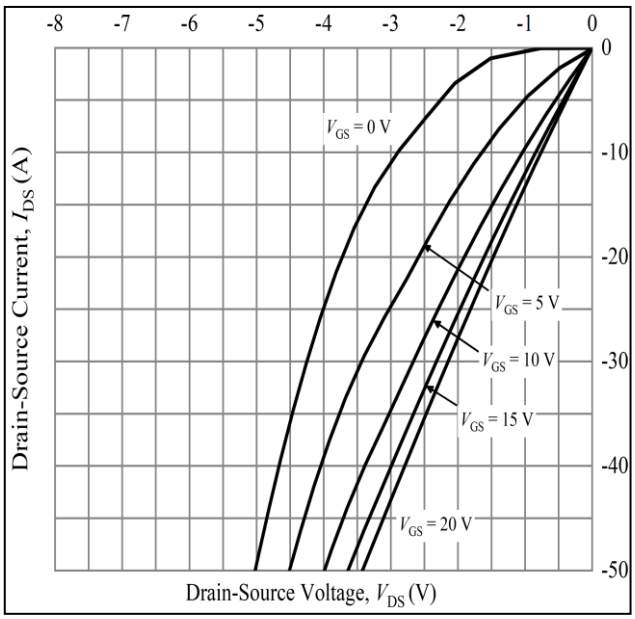


Figure 15: Typical 3rd Quadrant Characteristics at T_J = 175 °C

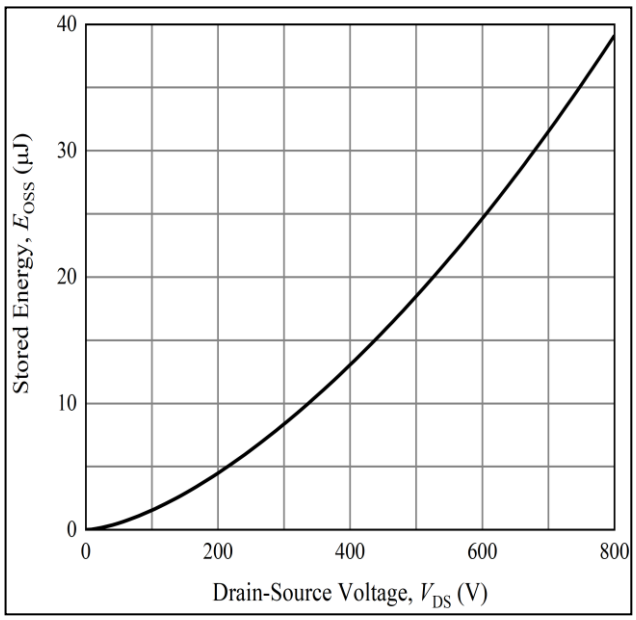


Figure 16: Typical Output Capacitor Stored Energy

Typical Performance

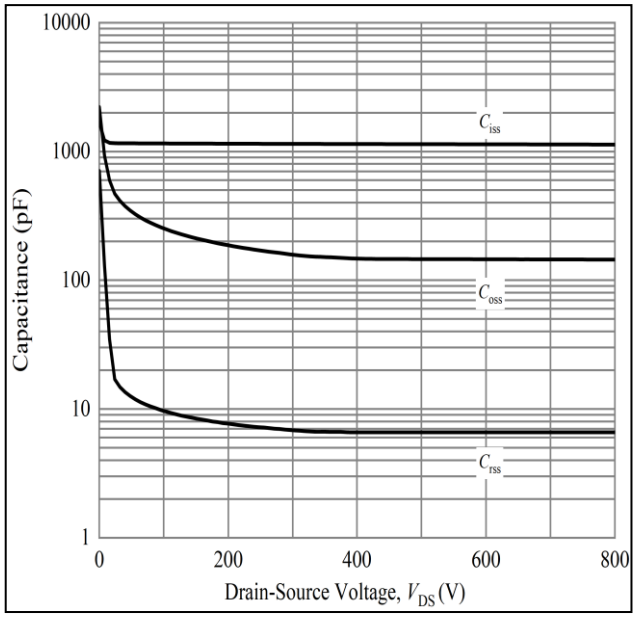


Figure 17: Typical Capacitances vs. Drain-Source Voltage

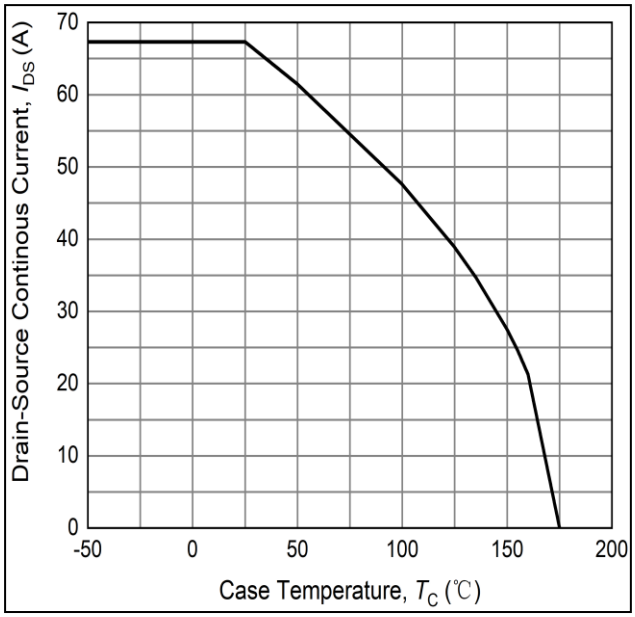


Figure 18: Continuous I_{DS} Current Derating Curve

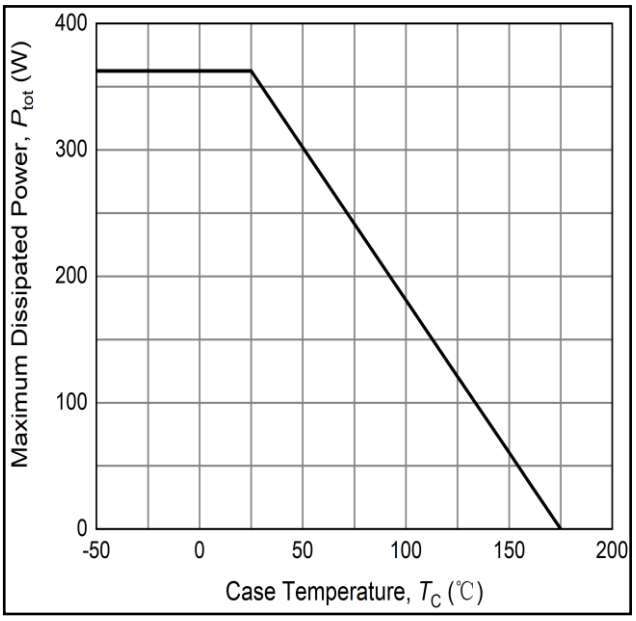


Figure 19: Power Dissipation Derating Curve

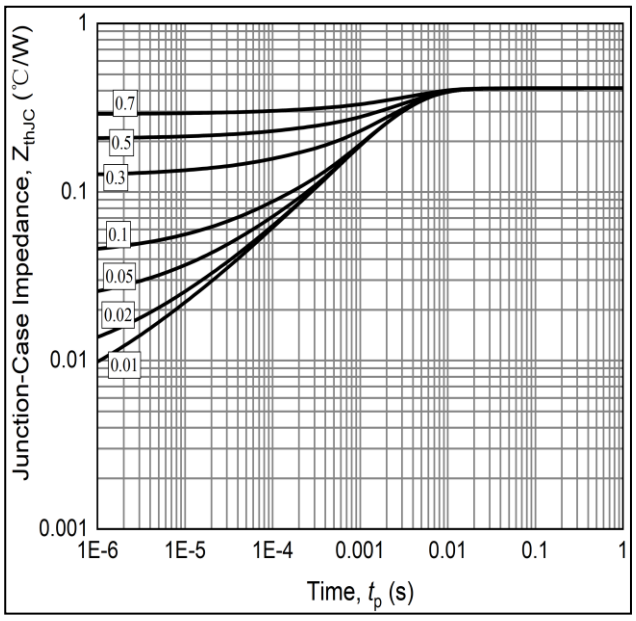


Figure 20: Typical Transient Thermal Impedance (Junction – Case) with Duty Cycle

Typical Performance

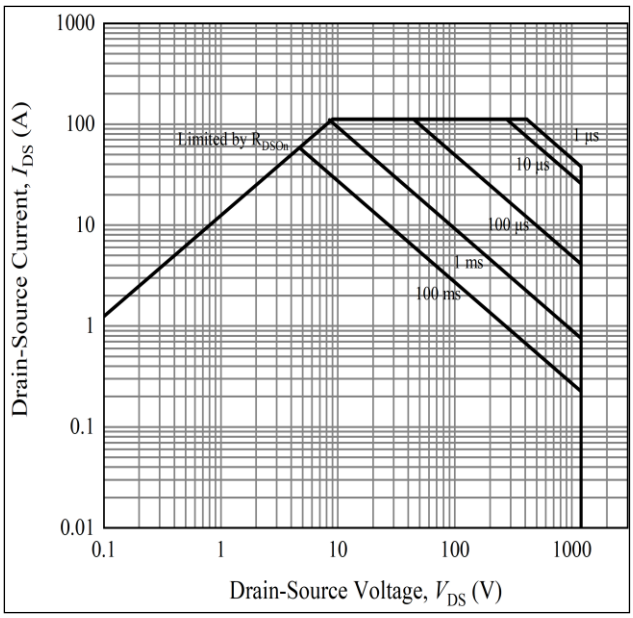


Figure 21: Safe Operate Area

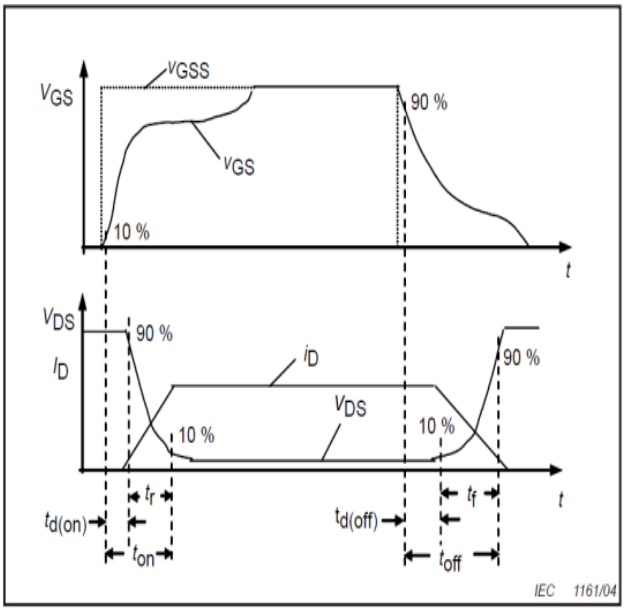


Figure 22: Resistive Switching Time Description

Test Circuit Schematic

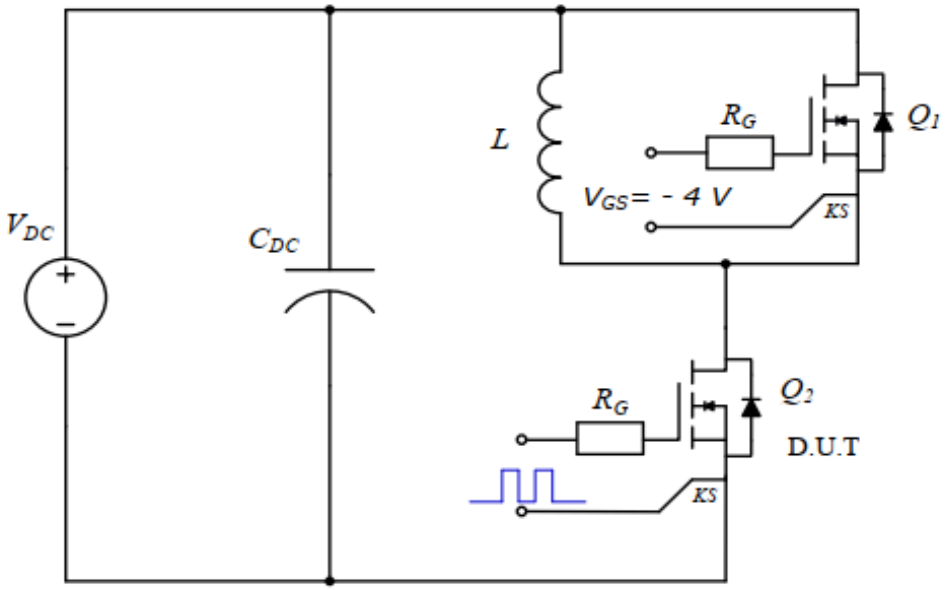
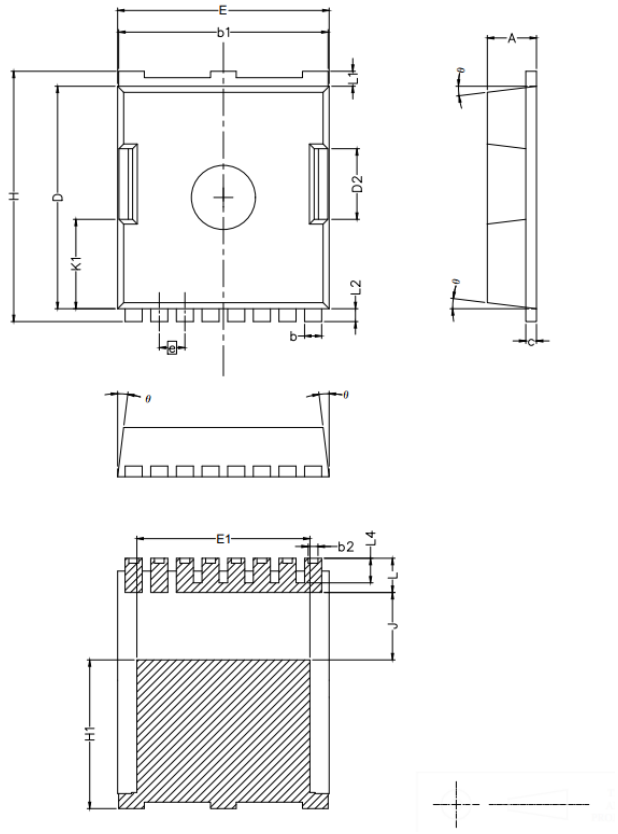


Figure 23: Clamped Inductive Switching Waveform Test Circuit

Package Dimensions

Package： TOLL



SYMBOL	MIN	MAX
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20 BSC	
H	11.48	11.88
H1	6.75	7.15
N	8	
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

4.0 RADIUS ON TERMINAL IS OPTIONAL.

Revision History

Document Version	Description of Changes
Rev.1.0	Released

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